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Effective on 12/8/2004.
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FEE TRANSMITTAL
For FY 2005

	Complete if Known
Application Number	09/836,065
Filing Date	04/16/2001
First Named Inventor	Naksrikram
Examiner Name	Chaudry, Mujtaba M.
Art Unit	2133
Attorney Docket No.	0180212 (Previously P1310)

☐ Applicant Claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT $500.00

METHOD OF PAYMENT (check all that apply)

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☒ Deposit Account Deposit Account Number: 50-0731 Deposit Account Name: Farjami & Farjami LLP

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 20 or HP =	0	x	$50.00	=	$ 0.00

HP = highest number of total claims paid for, if greater than 20

Indep. Claims		Extra Claims		Fee ($)		Fee Paid ($)
	- 3 or HP =	0	x	$200.00	=	$ 0.00

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
$360.00	

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41 (a)(1)(G) and 37 CFR 1.16(s).

Total Sheets		Extra Sheets		Number of each additional 50 or fraction thereof		Fee ($)		Fee Paid ($)
	- 100 =	0	/ 50 =	0	(round up to a whole number) x	$250.00	=	$ 0.00

4. OTHER FEE(S)

	Fees Paid($)
Non-English Specification, $130 fee (no small entity discount)	
Other: **Filing a brief in support of an appeal**	**$500.00**

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 38135	Telephone (949) 282-1000
Name (Print/Type)	Michael Farjami, Esq.		Date 4/8/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Art Unit: 2133
Naksrikram, et al.	Examiner: Chaudry, Mujtaba M.
Serial No.: 09/836,065	
Filed: April 16, 2001	
For: **System and Method for Erase Test of Integrated Circuit Device Having Non-Homogeneously Sized Sectors**	

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Honorable Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This is an Appeal from the Examiner's Final Rejection of claims 1-18. The Final Rejection issued on December 1, 2004. The Notice of Appeal was filed in the U.S. Patent and Trademark Office on March 1, 2005.

REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc.

RELATED APPEALS AND INTERFERENCES

There are no related Appeals or Interferences.

STATUS OF CLAIMS

Claims 1-18 are pending. Claims 1-18 have been finally rejected in a Final Rejection dated December 1, 2004. This Appeal is directed to the rejection of claims 1-18. Claims 1-18 appear in an Appendix to this Appeal Brief.

STATUS OF AMENDMENTS

No claim amendments were submitted in the response to the Final Rejection dated December 1, 2004.

SUMMARY OF CLAIMED SUBJECT MATTER

A. Claim 1

Independent claim 1 recites a method for testing a semiconductor device (e.g. a flash memory device) having a first sector (e.g. sectors 4-6) of a first sector type memory size (e.g. a uniformly sized sector) and a second sector (e.g. sectors 0-3) of a second sector type memory size (e.g. a boot sector), the method including measuring a first time

period (e.g. block 24 in Figure 3) related to erasing the first sector (e.g. sectors 4-6). Page 3, lines 25-31, page 4, lines 3 and 12-17, and Figures 1 and 3 of the present application. For example, boot sectors (e.g. sectors 0-3) are generally smaller (i.e. have a smaller number of memory cells) than the uniform sectors (e.g. sectors 4-6). Page 4, lines 3-4 of the present application. For example, uniformly sized sectors all have the same number of memory cells, while boot sectors may or may not have the same number of memory cells as each other. Page 3, lines 27-31 and page 4, lines 1-3 of the present application.

The method further includes establishing a first test limit (e.g. block 36 in Figure 4) based on the first time period. Page 5, line 1 and Figure 4 of the present application. As disclosed in the present application, the test limit is based on one or more, preferably both of: the average erase time period for sectors in the type, and the average auto program disturb erase (APDE) time period for sectors in the type. Page 5, lines 1-3. As disclosed in the present application, in one embodiment the test limit is defined to be 1.5 times the sum of the average erase time period plus the average APDE time period. Page 5, lines 3-5 of the present application. The method further includes measuring a second time period (e.g. block 24 in Figure 3) related to erasing the second sector (e.g. sectors 0-3). Page 4, line 17 and Figure 3 of the present application.

The method further includes establishing a second test limit (e.g. block 36 in Figure 4) based on the second time period. Page 5, line 1 and Figure 4 of the present application. The method further includes determining whether the device passes or fails an erase test (e.g. decision diamond 40 in Figure 4) by using the first test limit and the

second test limit during the erase test. Page 5, lines 7-16 and Figure 4 of the present application. As disclosed in the present application, it is determined whether either one or the sum of both of the sector's erase time period plus APDE time period exceed the test limit at decision diamond 40. Page 5, lines 7-9 and Figure 4 of the present application. As disclosed in the present application, preferably the sum of the sector's erase time period and APDE time period are compared to the test limit at decision diamond 40. Page 5, lines 9-10 of the present application. As disclosed in the present application, if the sum exceeds the limit, "FAIL" is returned at block 42 and device 10 (e.g. a flash memory device) is rejected. As disclosed in the present application, if a "FAIL" is not returned at block 42 before each sector of each type in device 10 has been evaluated, the test evaluation ends at state 48, which indicates that device 10 has passed the erase test. Page 5, lines 10-16 and Figure 4 of the present application.

Thus, the present invention, as defined by independent claim 1, advantageously achieves a method for testing a flash memory device having first and second sectors of respective first and second type memory sizes, where first and second test limits, which correspond to respective first and second sectors, are used to determine whether the device passes or fails an erase test. As a result, the present invention advantageously reduces the number of false rejects compared to a conventional approach that uses only a single test limit to test sectors having different sector type memory sizes. Page 2, lines 11-15 of the present application.

B. Claim 10

Independent claim 10 recites a system for testing a semiconductor device (e.g. a flash memory device) having a first sector (e.g. sectors 4-6) of a first sector type memory size (e.g. a uniformly sized sector) and a second sector (e.g. sectors 0-3) of a second sector type memory size (e.g. a boot sector), the system including a measuring element configured to measure a first time period (e.g. block 24 in Figure 3) related to erasing the first sector (e.g. sectors 4-6). Page 3, lines 25-31, page 4, lines 3 and 12-17, and Figures 1 and 3 of the present application. For example, boot sectors (e.g. sectors 0-3) are generally smaller (i.e. have a smaller number of memory cells) than the uniform sectors (e.g. sectors 4-6). Page 4, lines 3-4 of the present application. For example, uniformly sized sectors all have the same number of memory cells, while boot sectors may or may not have the same number of memory cells as each other. Page 3, lines 27-31 and page 4, lines 1-3 of the present application.

In the system recited in independent claim 10, the measuring element is further configured to measure a second time period (e.g. block 24 in Figure 3) related to erasing the second sector (e.g. sectors 0-3). Page 4, line 17 and Figure 3 of the present application. The system further includes an establishing element configured to establish a first test limit (e.g. block 36 in Figure 4) based on the first time period. Page 5, line 1 and Figure 4 of the present application. As disclosed in the present application, the test limit is based on one or more, preferably both of: the average erase time period for sectors in the type, and the average auto program disturb erase (APDE) time period for sectors in

the type. Page 5, lines 1-3. As disclosed in the present application, in one embodiment the test limit is defined to be 1.5 times the sum of the average erase time period plus the average APDE time period. Page 5, lines 3-5 of the present application. The establishing element is further configured to establish a second test limit (e.g. block 36 in Figure 4) based on the second time period. Page 5, line 1 and Figure 4 of the present application.

The system further includes a determining element configured to determine whether the device passes or fails an erase test (e.g. decision diamond 40 in Figure 4) by using the first test limit and the second test limit during the erase test. Page 5, lines 7-16 and Figure 4 of the present application. As disclosed in the present application, it is determined whether either one or the sum of both of the sector's erase time period plus APDE time period exceed the test limit at decision diamond 40. Page 5, lines 7-9 and Figure 4 of the present application. As disclosed in the present application, preferably the sum of the sector's erase time period and APDE time period are compared to the test limit at decision diamond 40. Page 5, lines 9-10 of the present application.

As disclosed in the present application, if the sum exceeds the limit, "FAIL" is returned at block 42 and device 10 (e.g. a flash memory device) is rejected. As disclosed in the present application, if a "FAIL" is not returned at block 42 before each sector of each type in device 10 has been evaluated, the test evaluation ends at state 48, which indicates that device 10 has passed the erase test. Page 5, lines 10-16 and Figure 4 of the present application. As disclosed in the present application, the erase test logic in Figure 3 and the erase test evaluation logic in Figure 4 can be embodied in a computer or other

digital processor that is programmed to execute method acts in accordance with the logic. Page 5, lines 17-18 of the present application.

Thus, the present invention, as defined by independent claim 10, advantageously achieves a system for testing a flash memory device having first and second sectors of respective first and second type memory sizes, where first and second test limits, which correspond to respective first and second sectors, are used to determine whether the device passes or fails an erase test. As a result, the present invention advantageously reduces the number of false rejects compared to a conventional approach that uses only a single test limit to test sectors having different sector type memory sizes. Page 2, lines 11-15 of the present application.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-18 stand rejected under 35 U.S.C. §103 as being unpatentable over U.S. Patent No. 5,343,434 to Kenji Noguchi (hereinafter "Noguchi") in view of U.S. Patent No. 5,646,948 to Kobayashi et al. (hereinafter "Kobayashi").

ARGUMENT

A. Rejection of claims 1-18 under 35 U.S.C. §103 over Noguchi in view of Kobayashi

For the reasons discussed below, Appellant respectfully submits that the present invention, as defined by independent claims 1 and 10, is patentably distinguishable over Noguchi and Kobayashi, singly or in combination thereof.

In contrast to the present invention as defined by independent claim 1, Noguchi does not teach, disclose, or suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. Noguchi is directed to a method for reducing the rate at which fail products are produced by use of a flash memory which is determined as fail because of the presence of an over-erased memory cell as a one-time programmable memory device. See, for example, the Abstract of Noguchi. Noguchi specifically discloses an erasing operation of a nonvolatile semiconductor memory device where, in an erase cycle, if memory cell data is unerased, an erase pulse width TEW is incremented and an erasing sequence is repeated. See, for example, column 7, lines 7-8, column 8, lines 9-11, and Figure 14 of Noguchi.

Thus, the erase operation disclosed in Noguchi includes erasing memory cells in a memory array. However, Noguchi fails to teach, disclose, or remotely suggest a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size, as specified in independent claim 1. In fact, Noguchi does not even mention different sectors in a memory device having different sector type memory sizes. Also, Noguchi fails to teach, disclose, or remotely suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test, as specified in independent claim 1.

As discussed above, by providing a method for testing a flash memory device having first and second sectors of respective first and second type memory sizes, where first and second test limits, which correspond to respective first and second sectors, are used to determine whether the device passes or fails an erase test, the present invention, as defined by independent claim 1, advantageously reduces the number of false rejects compared to a conventional approach that uses only a single test limit to test sectors having different sector type memory sizes. Thus, the method disclosed, taught, or suggested in Noguchi is substantially different than the method specified in independent claim 1.

In contrast to the present invention as defined by independent claim 1, Kobayashi does not teach, disclose, or suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. Kobayashi is directed to a memory testing apparatus which is capable of concurrently testing a plurality of semiconductor flash memories in parallel. See, for example, Kobayashi, column 1, lines 11-15. Kobayashi specifically discloses a semiconductor memory test apparatus comprising timing generator 10, pattern generator 2, waveform shaper 3, logical comparing part 40, and all-pass detector (NOR gate) 43, which are used for testing "n" flash memories MUT_1, MUT_2, ... MUT_n that are in "n" test channels, respectively. See, for example, column 4, lines 31-44 and Figure 1 of Kobayashi.

In Kobayashi, "n" flash memories MUT_1 to MUT_n are concurrently tested in "n" respective test channels. Thus, Kobayashi discloses concurrently testing "n" separate flash memories MUT_1 to MUT_n in parallel. However, Kobayashi fails to teach, disclose, or remotely suggest erase testing a semiconductor device having first and second sectors with respective first and second sector memory sizes, as specified in independent claim 1. In fact, Kobayashi fails to even a mention a semiconductor device having a first sector of

a first sector type memory size and a second sector of a second sector type memory size, as specified in independent claim 1.

As such, Kobayashi fails to teach, disclose, or even suggest measuring a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a second sector of a second type memory size, establishing a first test limit and a second test limit based on the respective first time period and second time period, and determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test, as specified by independent claim 1. Thus, Kobayashi fails to cure the basic deficiencies of Noguchi discussed above.

On pages 7 and 8 of the Final Rejection dated December 1, 2004, the Examiner states that incorporating the multiple memories of Kobayashi with the testing apparatus of Noguchi would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by applying the testing routine taught by Noguchi with multiple memory types would reduce overall testing time. However, considered together, the collective teachings of Noguchi and Kobayashi do not and cannot result in the present claimed invention. As discussed above, neither Kobayashi nor Noguchi teach, disclose, or remotely suggest using a first test limit to test first sectors having a first sector type memory size and using a second test limit to test second sectors having a second sector type memory size in an erase test for first and second sectors are in a semiconductor device, as specified in independent claim 1.

Moreover, as discussed above, Noguchi is directed to a method for reducing the rate at which fail products are produced by use of a flash memory which is determined as fail because of the presence of an over-erased memory cell as a one-time programmable memory device. In contrast, Kobayashi is directed to a memory testing apparatus which is capable of concurrently testing a plurality of semiconductor flash memories in parallel. Thus, the method of Noguchi is significantly different than the memory testing apparatus disclosed in Kobayashi. As such, Appellant respectfully submits that the purported teachings suggested by the Examiner (i.e. the combined teachings of Noguchi and Kobayashi) are not based on sufficient evidence of reason, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to make the suggested modifications.

For the foregoing reasons, Appellant respectfully submits that the present invention, as defined by independent claim 1, is not suggested, disclosed, or taught by Noguchi and Kobayashi, singly or in combination. As such, independent claim 1 is patentably distinguishable over Noguchi and Kobayashi. Thus, claims 2-9 depending from independent claim 1 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

The present invention, as defined by independent claim 10, includes, among other things, a measuring element configured to measure a first time period and a second time period related to erasing a respective first sector of a first sector type memory size and a

second sector of a second type memory size, an establishing element configured to establish a first test limit and a second test limit based on the respective first time period and second time period, and a determining element configured to determine whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test. Independent claim 10 includes similar limitations as independent claim 1 discussed above. Thus, for similar reasons as discussed above, independent claim 10 is also patentably distinguishable over Noguchi and Kobayashi. Thus, claims 11-18 depending from independent claim 10 are, *a fortiori*, also patentably distinguishable over Noguchi and Kobayashi for at least the reasons presented above and also for additional limitations contained in each dependent claim.

CONCLUSION

Based on the foregoing reasons, the present invention, as defined by independent claims 1 and 10 and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-18 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-18 pending in the present application is respectfully requested.

This Appeal Brief is submitted herewith with an Appendix of the appealed claims and the requisite fee for filing the Appeal Brief.

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Date: 4/8/05

Michael Farjami, Esq.
Reg. No. 38, 135

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

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Christina Carter 4/8/05
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APPENDIX OF CLAIMS ON APPEAL

Claim 1: A method for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size, the method comprising:

measuring a first time period related to erasing the first sector;

establishing a first test limit based on the first time period;

measuring a second time period related to erasing the second sector;

establishing a second test limit based on the second time period; and

determining whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test.

Claim 2: The method of Claim 1, wherein the semiconductor device comprises a plurality of first sectors and a plurality of second sectors, and the first test limit is based on an average of first time periods associated with the first time period for each of the first sectors and the second test limit is based on an average of second time periods associated with the second time period for each of the second sectors.

Claim 3: The method of Claim 1 further comprising:

measuring a third time period related to erasing the first sector; and

measuring a fourth time period related to erasing the second sector, the first and second time periods being erase time periods; and the third and fourth time periods being auto program disturb erase time periods, the first test limit being based on at least one of the first and third time periods; the second test limit being based on at least one of the second and fourth time periods.

Claim 4: The method of Claim 3, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 5: The method of Claim 2 further comprising:

measuring a third time periods related to erasing each of the plurality of first sectors; and

measuring a fourth time periods related to erasing each of the plurality of second sectors, the first and second time periods being erase time periods; and the third and fourth time periods being auto program distrub erase time periods, the first test limit being based on at least one of the first and third time periods; the second test limit being based on at least one of the second and fourth time periods.

Claim 6: The method of Claim 5, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 7: The method of Claim 1, wherein the act of determining includes determining whether a time period associated with erasing the first sector exceeds the first test limit and whether a time period associated with erasing the second sector exceeds the second test limit.

Claim 8: The method of Claim 1, further comprising executing at least one parameter test on the device, wherein said at least one parameter test is selected from the group consisting of a test for open circuits, a test for short circuits, a test for electrical leakage, and a device signature test.

Claim 9: The method of Claim 1, wherein the second sector is a boot sector.

Claim 10: A system for testing a semiconductor device having a first sector of a first sector type memory size and a second sector of a second sector type memory size, the system comprising:

a measuring element configured to measure a first time period related to erasing the first sector, the measuring element further configured to measure a second time period related to erasing the second sector;

an establishing element configured to establish a first test limit based on the first time period, the establishing element further configured to establish a second test limit based on the second time period; and

a determining element configured to determine whether the device passes or fails an erase test by using the first test limit and the second test limit during the erase test.

Claim 11: The system of Claim 10, wherein the device comprises a plurality of first sectors and a plurality of second sectors, and the first test limit is based on an average of first time periods associated with the first time period for each of the first sectors and the second test limit is based on an average of second time periods associated with the second time period for each of the second sectors.

Claim 12: The system of Claim 10, wherein the measuring element is further configured to measure a third time period related to erasing the first sector and a fourth time period related to erasing the second sector, and wherein the first and second time periods being erase time periods and the third and fourth time periods being auto program disturb erase time periods; the first test limit being based on at least one of the first and

third time periods; the second test limit being based on at least one of the second and fourth time periods.

Claim 13: The system of Claim 12, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 14: The system of Claim 11, wherein the measuring element is further configured to measure a third time period related to erasing each of the plurality of first sectors and a fourth time period related to erasing each of the plurality of second sectors, the first and second time periods being erase time periods and the third and fourth time periods being auto program disturb erase time periods; the first test limit being based on at least one of the first and third time periods; the second test limit being based on at least one of the second and fourth time periods.

Claim 15: The system of Claim 14, wherein the first test limit is based on both of the first and third time periods, and the second test limit is based on both of the second and fourth time periods.

Claim 16: The system of Claim 10, wherein the determining element determines whether a time period associated with erasing the first sector exceeds the first test limit

and whether a time period associated with erasing the second sector exceeds the second test limit.

Claim 17: The system of Claim 10, wherein the system executes at least one parameter test on the device, wherein said at least one parameter test is selected from the group consisting of a test for open circuits, a test for short circuits, a test for electrical leakage, and a device signature test.

Claim 18: The system of Claim 10, wherein the second sector is a boot sector.